REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1, 4-7, 9-12, 15-18 and 20-22 remain active in this, Claims 1, 6, 7,11, 12, 17, 18, and 22 having been amended by the present amendment and Claims 2, 3, 8, 13, 14 and 19 having previously been canceled.

In the outstanding Official Action, Claims 1, 4-7, 9-12, 15-18 and 20-22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Yano (U.S. Patent No. 6,118,165).

In light of the outstanding ground for rejection, the pending claims have been amended to clarify what is believed to be a clearly patentably distinguishing feature. To that end, Claim 1, for example, has been amended to state that --a sum of areas of said surface portions of said semiconductor layer receiving incident light being larger than a sum of areas of said plurality of first semiconductor regions and said second semiconductor region.-- Thus, as is evident from amended Claim 1, light is mainly incident on the area between each of the plurality of first semiconductor regions and the second semiconductor region without passing through these semiconductor regions. Therefore, it is possible to use the incident light to the semiconductor light-receiving device effectively without absorption of the incident light in the semiconductor regions. Further, the areas between the first and second semiconductor regions have higher resistances than resistances of the first and second semiconductor regions and are completely depleted in a state in which a reverse bias is applied between the first and second electrodes, so that the sensitivity characteristics of the device can be made superior.

In addition, as stated in amended Claim 1, the plurality of first semiconductor regions are formed apart from each other, and the second electrode are formed on the second surface

of the semiconductor substrate and not formed on the first semiconductor regions. Therefore, an area for contact to the second electrode is not necessary on each of the plurality of first semiconductor regions so that it is possible to narrow a top surface area of the plurality of first semiconductor regions. This results in widening an area between each of the plurality of first semiconductor regions and the second semiconductor region, which is a light-receiving surface, as recited in amended Claim 1, to increase amount of light incident to the semiconductor light-receiving device.

Similar changes as above noted with respect to Claim 1 have been made to the other independent Claims 7, 12, and 18. According to the claimed invention defined by each pending independent claim, it is possible to obtain the above-mentioned effects.

Turning now to the outstanding ground for rejection, this rejection is based on the finding that the Applicant's Prior Art (Fig. 7) discloses the present invention except for the second electrode formed on the second side and Yano discloses a light-receiving device containing a photodiode one electrode of which is formed on the second side.

However, in the semiconductor light-receiving device of the Applicant's Prior Art (Fig. 7), an N-type epitaxial layer 74 is disposed under plural N-type diffusion regions 76, and areas of regions between the plural N-type diffusion regions 76 and a P-type separating diffusion region 75 are very narrow. In the semiconductor light-receiving device of Fig. 7, light is mainly incident into the N-type epitaxial layer 74 through the plural N-type diffusion regions 76. This results in decreasing an amount of incident light which passes these regions into the N-type epitaxial layer 74. A large amount of incident light is absorbed in the plural N-type diffusion regions 76 and the P-type separating diffusion region 75. Therefore, it is impossible to use the incident light to the semiconductor light-receiving device effectively, so that a sufficient sensitivity cannot be obtained.

Further, an electrode for giving a substrate potential 83 is provided on the P-type separating diffusion region 75 and not on the other side of the P-type semiconductor substrate 81. Therefore, a large area for contact to the electrode 83 is necessary on the P-type separating diffusion region 75 considering a shift margin of forming the electrode 83, so that it is impossible to narrow a top surface area of the P-type separating diffusion region 75. This results in narrowing of an area of the N-type epitaxial layer 74 between the P-type separating diffusion region 75 and each of the plural N-type diffusion regions 76 thereby to decrease amount of light incident to the semiconductor light-receiving device.

Yano also does not teach the above-mentioned features of the claimed invention and does not cure the deficiencies of the admitted prior art so that the advantages of the claimed invention can not be derived, absent hindsight, from the teachings of the applied prior art.

Indeed, in the semiconductor light-receiving device of the Applicant's admitted prior art (Fig. 7 which is a cross-sectional view of the attached Fig. A along a line A-A'), which corresponds to Japanese Patent Laid-Open No. 270744/1998, a P-type separating diffusion region 75 is disposed such that the region 75 electrically separates an N-type epitaxial layer 74 into plural light detecting regions D1, D2, D3, D5 (see the attached Fig. A which is a plan view of the device of Fig. 7). Each of the plural light detecting regions D1, D2, D3, D5 corresponds to a photodiode. The region 75 surrounds each of the plural different light detecting regions D1, D2, D3, D5. Each of plural N-type diffusion regions 76 is formed apart from each other and disposed corresponding to each of the regions D1, D2, D3, D5. In other words, each of the plural N-type diffusion regions 76 is surrounded by the P-type separating diffusion region 75 (see the attached Fig. B which is a perspective side view of the device of Fig. 7). The arrangement of the P-type separating diffusion region 75 and the plural N-type diffusion regions 76 is reverse to those of the plurality of first semiconductor regions and the second semiconductor region in the claimed invention.

In the claimed invention, on the other hand, the second semiconductor region has a lattice form or a network form to surround each of the plurality of first semiconductor regions with surface portions of the semiconductor layer therebetween, and further the first electrode has a lattice form or a network form (see Figs. 1A, 3A, 4A, 5A, 6A of Applicant's disclosure). These features of the present invention are not disclosed in the admitted prior art (Fig. 7), and are not believed to be remedied by Yano.

Consequently, in view of the present amendment and in light of the above discussion, it is respectfully submitted that the amended claims patentably define over the cited references and are in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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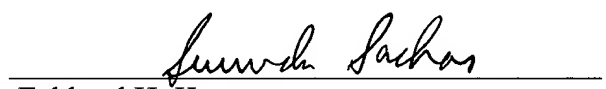

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